Custom Analog VLSI for the Advanced Composition Explorer (ACE)

W. R. Cook, A. Cummings, B. Kecman, R. A. Mewaldt (Caltech, Pasadena CA 91125)
D. Aalami (Space Instruments, Mission Viejo CA 92691)
S. A. Kleinfelder (VLSI Physics, Berkeley CA 94705)
J. H. Marshall (MDH Industries, Inc., Monrovia CA 91016)

ABSTRACT

Two custom analog VLSI chips are currently in development for scientific payloads of NASA's Advanced Composition Explorer. One chip will be fabricated in the radiation hard 1.2 um CMOS process of the United Technologies Microelectronics Center (UTMC), and will contain 16 complete discriminator/12 bit pulse-height-analysis chains for the readout of heavy ion Si strip detectors. The second chip will be fabricated by Harris Semiconductor in their dielectrically isolated bipolar VHF process. This chip will contain the active elements of a single precision pulse-height-analysis chain and several precision discriminator chains. The chips designed in this effort and the techniques employed are expected to be applicable in science payloads of future missions, especially those which place extraordinary premiums on weight, power, and/or performance.

I. Introduction

Our development of custom CMOS VLSI circuitry for the readout of heavy ion silicon strip detectors has been motivated by the planned use of such detectors in the Solar Isotope Spectrometer (SIS) of NASA's Advanced Composition Explorer (ACE), together with the successful implementation of similar VLSI readout circuitry for use in high energy physics experiments. (See e.g., Kleinfelder et al. 1988 and Kleinfelder 1989). SIS incorporates silicon strip detectors to measure the trajectory and dE/dx of incident nuclei. The high rate of incident nuclei expected during large solar flares requires the separate readout of individual detector strips to avoid pileup that would result if charge division techniques were employed. Thus each of the 512 detector strips in SIS needs a moderately high precision (11-12 bits) pulse height analysis (PHA) chain. In this application, the custom CMOS VLSI readout under development will yield a large reduction in weight and a moderate reduction in power relative to a conventional readout approach, while greatly reducing parts count and complexity.

In addition, after reviewing the commercially available VLSI technologies it was clear that existing discrete bipolar designs of general purpose precision PHA and amplifier/discriminator chains could be ported into a bipolar VLSI technology, provided that critical gain determining and bypass components were left off-chip. Such precision PHA and discriminator chains are needed in sufficient quantities in ACE to make the power, weight and parts count reductions offered by the VLSI approach very attractive. Hence, a second development effort was initiated. The expected performance and current status of the CMOS and bipolar circuits under development are briefly discussed below.

II. CMOS Heavy Ion Strip Detector Readout

The CMOS VLSI circuit under development contains 16 complete PHA/discriminator chains, each consuming about 20 mW. The design differs from previous similar ones in combining (1) asynchronous event capability, (2) a low gain (700 MeV in Si

full scale) suitable for the relatively large signals produced by heavy ions, (3) 12 bit resolution, and (4) a novel method of handling detector leakage current.

Each PHA/discriminator chain (see Figure 1) contains a charge sensitive preamplifier, a postamplifier/discriminator, a sample/hold section, and a 12 bit Wilkinson analog to digitial converter. During the period between asynchronously occurring charged particle hits, the preamp baseline output voltage (buffered by a precision follower) is alternately sampled onto hold capacitors C2 and C3, once every 3 usec. When a charge impulse due to an incident nucleus occurs, the preamp output steps to a new level with approximately a 100 ns time constant. This transition enters a shaping amplifier which produces a pulse with peak time near 500 ns that is presented to a discriminator. The externally adjustable discriminator threshold will be set near 3.5 MeV. The digital outputs of discriminators in all 16 channels are logically OR'ed to form a single trigger signal which is delivered off-chip to external control logic.

Under the control of this external logic and in parallel for all 16 chains, the process of sampling the preamp baseline onto C2 and C3 is halted, leaving a valid pre-trigger sample on either C2 or C3 which is then connected to the reference input of the Wilkinson comparator. The final post-trigger preamp output voltage level is sampled onto C1. The input charge amplitude is then found by measuring the time required to linearly ramp the voltage on C1 to the Wilkinson comparator reference voltage. To ensure this "rundown" time is non-zero for very small input signals a pedestal voltage is applied via C4 before beginning the ramp.

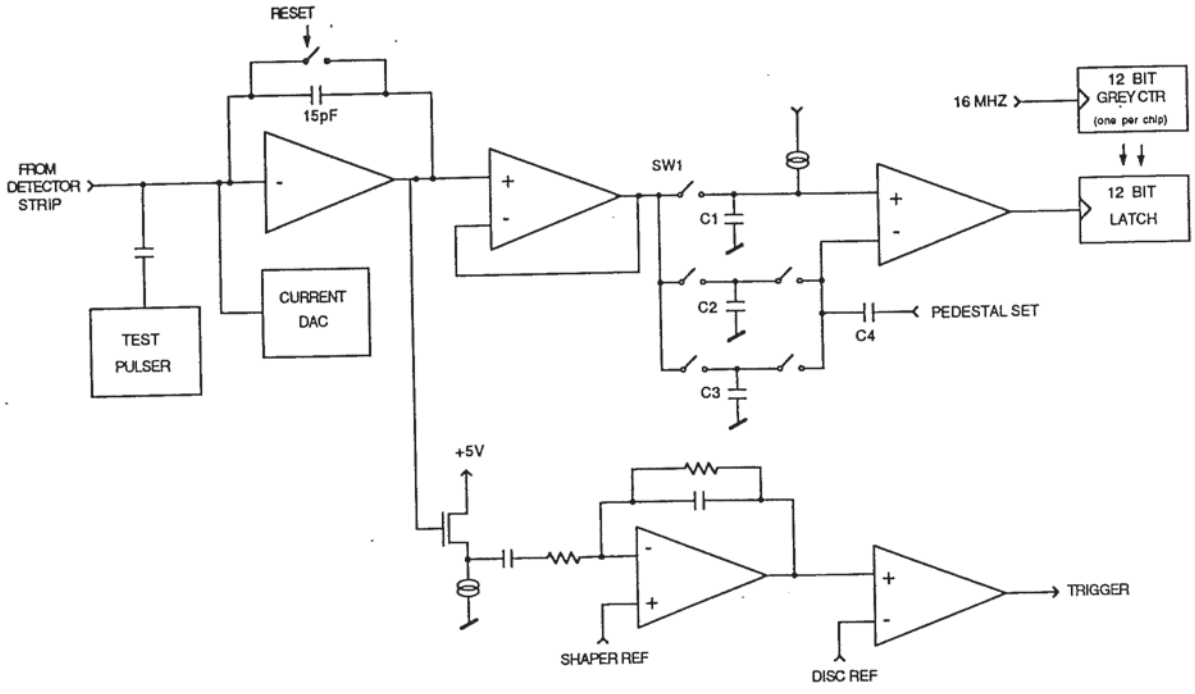

Figure 1: Heavy Ion Strip Detector Readout

The logical OR of all the Wilkinson comparator output signals is driven off chip to allow external logic to determine when all conversions are complete and to provide a relatively prompt indication of the size of the largest of the signals detected by the sixteen chains. After the completion of the longest rundown the pulse height data from the sixteen chains are read out through a single serial port, and the preamp voltages are reset.

The preamp inputs are intended to be DC coupled to the detector strips. Detector leakage current and any current which may flow between adjacent strips due to preamp input voltage mismatch will be approximately canceled by individually programmable current output DACs attached to the preamp inputs. This leakage current nulling controls the effect of leakage currents on the pulse height measurements and allows extension of the time between periodic preamp resets. Digital data which sets the individual DAC current levels will be downloaded from an external system microprocessor via a single on-chip serial command loop. The appropriate DAC levels will be determined by periodically (less than once per minute) performing a leakage current measurement cycle wherein the preamps are allowed to integrate for an extended period (about 500 usec). An important side benefit of these leakage current measurements will be to aid in monitoring detector health, both pre and post launch.

Other features of the VLSI design include on-chip test pulsers, the ability to disable individual chains (as may be needed in the case of a noisy strip), and configurability to handle both positive and negative polarity input signals. The later feature allows the same chip design to be used on either side of two-dimensional position sensitive strip detectors such as those planned for SIS.

This CMOS VLSI development has benefited from inexpensive prototyping through MOSIS. To date, prototypes of the key analog circuits have been tested both separately and as a complete PHA chain. A prototype having the analog components of 8 complete PHA chains is currently being fabricated through MOSIS, while the chip with the full complement of 16 PHAs is being laid out for final fabrication in the radiation hard 1.2 um process of UTMC.

III. Precision Bipolar PHA and Discriminator Chains

The bipolar VLSI chip under development will contain the active and non-critical passive components of a single precision low power pulse height analysis chain and an amplifier/dual-discriminator chain. The new VLSI designs represent an evolution of existing discrete bipolar transistor designs which have been flight proven in numerous space instruments over the past twenty-five years. (See Franzgrote and Marshall 1964, Halpern, Marshall and Weeks 1968, Halpern and Marshall 1968, Harrington and Marshall 1968, 1969, Marshall 1970, Harrington et al. 1974, Althouse et al. 1978, and Cook et al. 1993). The transfer and updating of these proven designs to VLSI technology promises improved performance, significant reductions in size, weight and power, as well as enhanced reliability and lower cost through greatly reduced part counts. The bipolar development is being done using the Fastrack system for fabrication in the Harris VHF process, which provides radiation tolerance to about 100 kRad. The development method relies heavily on detailed numerical simulation of circuit operation and performance, together with the guarantee by Harris of simulation fidelity.

Pulse amplitude measurements in the charged particle instruments of ACE require precision at the 0.1% level and a wide dynamic range to cover incident nuclei from helium to zinc. Thus, the design goal for the PHA chain is 12-13 bit resolution and linearity, with a dynamic range of 750. Offset stability of better than 0.5 LSB over -20 to 40 degrees C and

gain stability of less than 50 ppm per degree C are desired. Numerical circuit simulations, backed up by analytical calculations, indicate that these design goals will be met or surpassed. In particular, the self triggering PHA system is expected to (1) have a dynamic range approaching 3000, more than a three-fold increase relative to the prior discrete bipolar design, (2) achieve excellent linearity, with the maximum deviation of the transfer function from a best straight-line fit being less than 0.005% of full scale over the entire dynamic range, and (3) consume only 40 mW of power, an approximately three-fold reduction relative to the prior discrete design.

To reduce the requirements on the VLSI chip, we have chosen to put critical gain and offset determining passive components off chip. This also has the advantage of allowing the chip to service a wide range of applications. The basic configuration employs the on-chip preamplifier with a bipolar input for optimum noise performance at low power when used with room temperature detectors of relatively high capacitance and leakage current. A wide range of different detector properties and full scale amplitudes, as well as both input signal polarities, may be accommodated by the choice and arrangement of a few external feedback and compensation components. For low capacitance, low noise applications, such as Ge and Si detector spectroscopy, a high gain preamplifier configuration is available which employs an external FET that may be optimized for particular detector capacitance and performance needs.

For ACE applications, we plan to package the VLSI chip and associated passive components into two types of hybrids, one containing a PHA system and the other a small number of amplifier/discriminator systems. The resulting systems will be much smaller than previous ones. For example, the prior discrete bipolar PHA was packaged in six hybrids occupying a total area of approximately 100 sq. cm. The new PHA will occupy approximately 10 sq. cm, for a ten fold reduction.

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